MLSI-BPA82, BPA84, BPA84-A, BPA84-T, and BPA84-A-T BACKPLANE/CARD GUIDE ASSEMBLIES

For use with DEC™ LSI-11™ Computers

INSTRUCTION MANUAL

MDB SYSTEMS, INC.

MLSI-BPA82, BPA84, BPA84-A, BPA84-T, and BPA84-A-T BACKPLANE/CARD GUIDE ASSEMBLIES

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INSTRUCTION MANUAL

MDB SYSTEMS INC.
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INTRODUCTION

This is a technical manual for the five MDB backplane/card guide assemblies to be used with Digital LSI-11 Q-bus computers. The MLSI-BPA82, MLSI-BPA84, MLSI-BPA84-A, MLSI-BPA84-T, and MLSI-BPA84-A-T Backplane/Card Guide Assemblies are all wired for standard LSI-11 Q-bus signals. All backplanes are equipped with 22-bit addressing capabilities, although they will accommodate modules with 16-bit or 18-bit addressing.

PRODUCT DESCRIPTION

MLSI-BPA82 (P/N 40040334)

This pre-wired, printed circuit LSI-11 backplane/card guide assembly provides eight (8) standard Q-bus dual slots that will accommodate one (1) LSI-11/2 or LSI-11/23 microprocessor and seven (7) dual-size modules. All available slots have integral 22-bit addressing.

NOTE: When using an LSI-11/2 (KD11-HA) processor, the user should disable the 22-bit addressing lines from the processor. To disable 22-bit addressing, the etched jumpers at location B1 must be cut. (Refer to Figure 5 for jumper locations.)

The MLSI-BPA82 provides 22-bit bus termination by means of three (3) removable/pluggable 120 ohm resistor packs installed on the rear of the backplane. Also provided are terminal posts for standard LSI-11 and custom power requirements. Full-length card guides ensure maximum support for the installed modules.

The overall dimensions of the MLSI-BPA82 Backplane/Card Guide Assembly are as follows:

Height	Width	Depth	Weight
4.75" (12.06 cm)	7.30" (18.54 cm)	10.50" (26.67 cm)	3.0 lbs. (1.36 kg)

MLSI-BPA84-T (P/N 40040328)

This pre-wired, multilayer, printed circuit LSI-11 backplane/card guide assembly provides sixteen (16) dual or eight (8) quad standard Q-bus slots. These slots will accommodate a total of 16 dual-size modules (one LSI-11/2 or LSI-11/23 microprocessor and 15 dual-size modules), 8 quad-size modules, or a user-selected combination of both dual and quad-size modules. This backplane may also be used with the older DEC LSI-11 (KD11-F) microprocessor. All available slots have integral 22-bit addressing capabilities.

When using a KD11-F or KD11-HA processor, the 22-bit addressing lines should be user-disabled. (Refer to the NOTE above, and to Figure 6 for jumper locations.)

The MLSI-BPA84-T is also provided with removable/pluggable 120 ohm bus termination. This integral 22-bit termination is accomplished by means of two (2) small printed circuit boards on the rear of the backplane at slot 8 A-B. The MLSI-BP Adapter Module is factory-

soldered onto the backplane pins of slot 8 A-B, and the MLSI-QTA11 Plug-In Terminator Module is simply connected to it. The MLSI-BP Adapter is supplied with the appropriate female connector into which the MLSI-QTA11 mounts. The connection of these two printed circuit boards provides the required 120 ohm Q-bus termination. (For the location and installation of the MLSI-BP Adapter/QTA11 Terminator Assembly, refer to Figure 1 on the following page.)

The MLSI-BPA84-T also provides terminal posts for standard LSI-11 and custom power requirements. Full-length card guides ensure maximum support for the installed modules.

The overall dimensions of the MLSI-BPA84-T Backplane/Card Guide Assembly are as follows:

Height	Width	Depth	Weight
4.75" (12.06 cm)	12.56" (31.90 cm)	10.50" (26.67 cm)	5.0 lbs. (2.27 kg)

MLSI-BPA84 (P/N 40040335)

This backplane/card guide assembly is identical to the MLSI-BPA84-T, except for removable/pluggable 120 ohm bus termination, which is NOT provided on the MLSI-BPA84. Bus termination must be accomplished by means of an appropriate bus terminator module (i.e., MLSI-TEV-003 or equivalent).

NOTE: The MLSI-BP Adapter Module is not included on this backplane. Refer to Figure 1 on the following page.

MLSI-BPA84-A-T (P/N 40040329)

This pre-wired, multilayer, printed circuit LSI-11 backplane/card guide assembly is identical to the MLSI-BPA84-T, except for slots 6 and 7, in which the C-D portion has been specially wired to accept the DEC RLV11 and RLV21 Hard Disk Controllers. Power and ground are the only signals present on these slots; therefore, no other modules, including Bus Grant Continuity Cards (MLSI-BGC or equivalent), should be installed in dedicated slots 6 C-D and 7 C-D.

NOTE: Slots 6 A-B and 7 A-B may be used for dual-size or quad-size modules, providing the module in question has been designed with Q-bus connection requirements on the A and B portions only.

Another variation between the MLSI-BPA84-A-T and the MLSI-BPA84-T concerns the procedure for disabling the 22-bit addressing lines when using a KD11-F (LSI-11) or KD11-HA (LSI-11/2) microprocessor. To disable 22-bit addressing, the following wire jumpers must be removed:

5C1 - 8C1 5D1 - 8D1 5E1 - 8E1 5F1 - 8F1

Document Part Number: 80033328
Document Revision Level: B

The postage-prepaid READER'S COMMENTS page at the end of this instruction manual requests the user's critical evaluation to assist us in preparing future documentation.

Price: $10.00

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MLSI-BPA84-A (P/N 40040336

This backplane/card guide assembly is identical to the MLSI-BPA84-A-T, except for removable/pluggable 120 ohm bus termination, which is NOT provided on the MLSI-BPA84-A. Bus termination must be accomplished by means of an appropriate bus terminator module (i.e., MLSI-TEV-003 or equivalent). (Refer to the NOTE on the preceding page concerning the MLSI-BPA84 Backplane/Card Guide Assembly.)

INSTALLATION

The backplane/card guide assemblies may be mounted in either a horizontal or vertical plane, depending upon user requirements. Horizontal mounting can be accomplished in a 5.25" (13.34 cm) high chassis assembly. Mounting nuts are also contained in the bottom rails of the backplane to facilitate vertical mounting.

Slot 1 of the backplanes can be easily identified as the slot closest to the +12 V terminal post. The remainder of the backplane slots follow sequentially.

Figure 1 below shows an installation diagram of the MLSI-BP Adapter/QTA11 Terminator Assembly, which is supplied on the MLSI-BPA84-T and MLSI-BPA84-A-T Backplane/Card Guide Assemblies only.

FIGURE 1
INSTALLATION DRAWING: MLSI-BP ADAPTER/QTA11 TERMINATOR ASSEMBLY

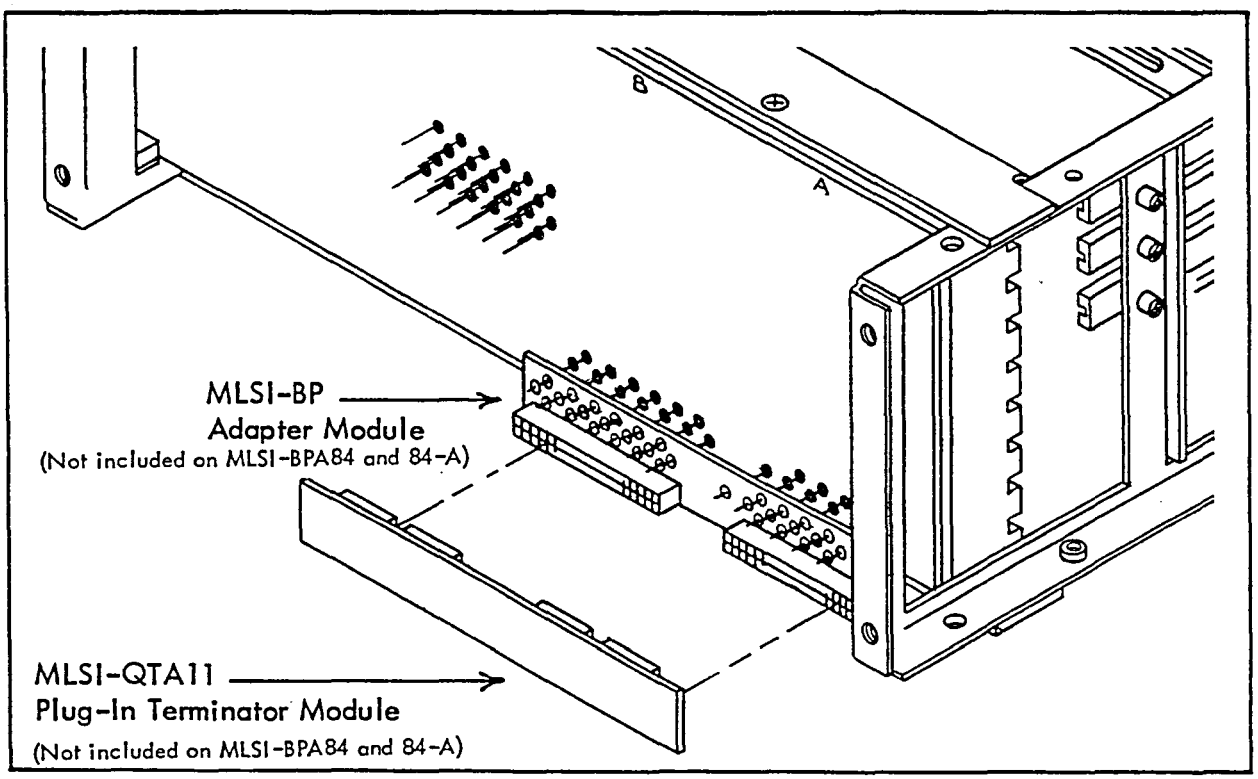
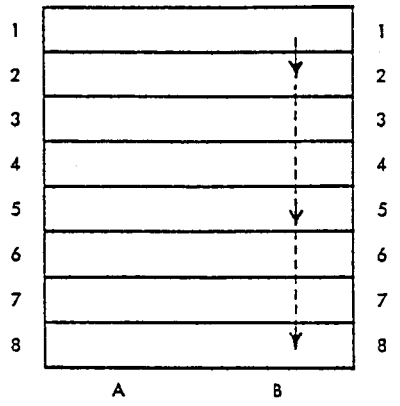
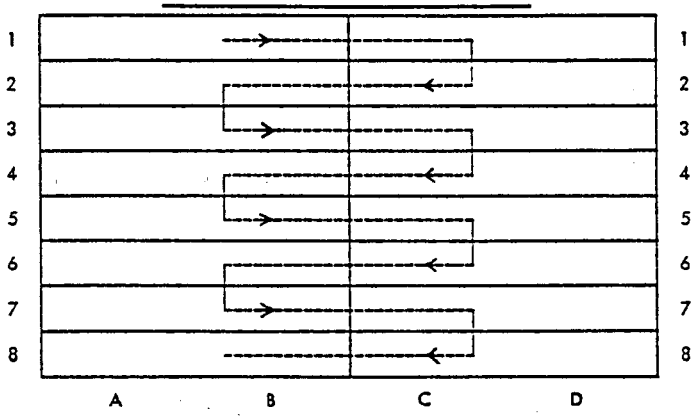


FIGURE 2
BACKPLANE CONFIGURATIONS

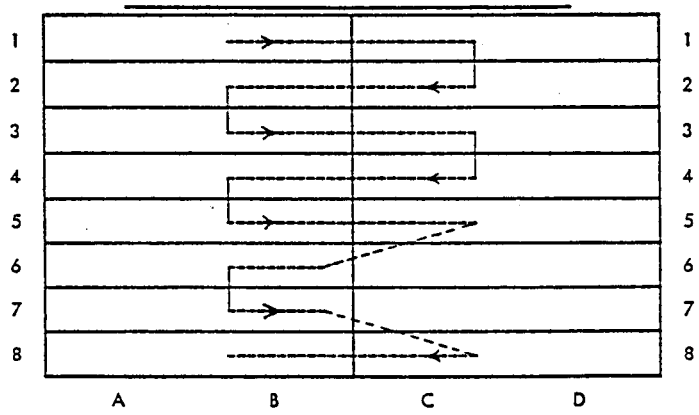
MLSI-BPA82



MLSI-BPA84 and BPA84-T



MLSI-BPA84-A and BPA84-A-T



Slots 6 C-D and 7 C-D are used for the DEC RLV11 and RLV21 Hard Disk Controllers.

APPLICATION NOTES

1: Chassis are shown as viewed from the front (module plug-in) side of chassis with the component sides of the modules facing up.

2: Dashed lines for the MLSI-BPA84-T and MLSI-BPA84-A-T show the Q-bus priority daisy chain sequence. Module placement should follow sequential slots. Priority for modules is dependent upon closeness to the CPU.

3: If it is necessary to leave an open slot in the priority daisy chain, a Bus Grant Continuity Card (MLSI-BGC or equivalent) must be inserted in the A and C portion only of the vacant slot. These devices will transfer the DMA and Interupt Bus Grant onto the next circuit board in the sequence.

FIGURE 3
MLSI-BPA84-T AND MLSI-BPA82 BACKPLANE CONFIGURATIONS

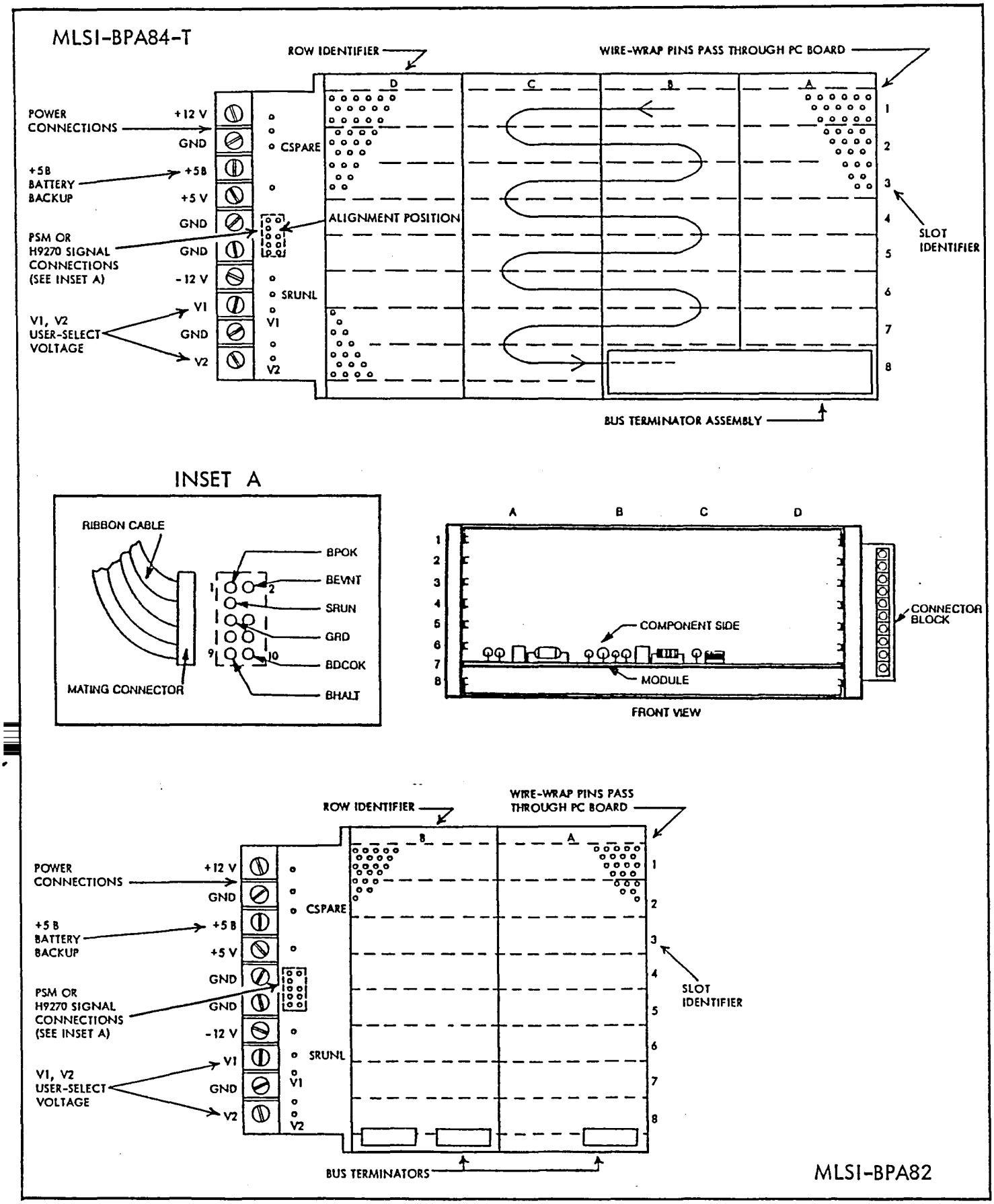


Table 1 lists and defines the signals and pin designations present at the LSI-11 Q-bus backplane.

TABLE 1
FUNCTIONAL DESCRIPTION OF Q-BUS SIGNALS

NOTE: When the MLSI-BPA82 Backplane is utilized, the pin designations listed in parentheses (C and D) do not apply.

Bus Pin	Mnemonic	Description
AA1 (CA1)	BIRQ5L	Priority Level 5 interrupt request.
AB1 (CB1)	BIRQ6L	Priority Level 6 interrupt request.
AC1 (CC1)	BDAL16L	Extended address bit 16.
AD1 (CD1)	BDAL17L	Extended address bit 17.
AE1 (CE1)	SSPARE	Spare pin. Not assigned. This pin is available for user connection.
AF1 (CF1)	SRUNL	Run light signal.
AH1 (CH1)	SRUNL	Run light signal.
AJ1 (CJ1)	GND	Signal ground.
AK1 (CK1)	MSPAREA	Maintenance spare. Normally connected to bus pin AL1 (CL1) on the backplane.
AL1 (CL1)	MSPAREA	Maintenance spare. Normally connected to bus pin AK1 (CK1) on the backplane.
AM1 (CM1)	GND	Signal ground.
AN1 (CN1)	BDMRL	Direct Memory Access (DMA) Request. Asserted by a device to request control of the bus (bus master). If the processor is not the bus master, and it is not asserting BSYNCL, it grants bus master status to the requesting device by asserting BDMGOL. The requesting device responds by negating BDMRL and asserting BSACKL.
AP1 (CP1)	BHALTL	Processor Halt. A device will cause the processor to halt normal program execution by asserting BHALTL.

TABLE 1
FUNCTIONAL DESCRIPTION OF Q-BUS SIGNALS (cont.)

Bus Pin	Mnemonic	Description
AR1 (CR1)	BREFL	Memory Refresh. When BREFL is asserted, the processor will perform as memory refresh that forces all dynamic memory devices to be activated for each BSYNCL/BDINL bus transaction.
AS1 (CS1)	+12B	+12V battery power.
AT1 (CT1)	GND	Signal ground.
AU1 (CU1)	PSPARE	Power Spare. Not assigned. This pin is not recommended for use.
AV1 (CV1)	+5B	+5V battery power.
AA2 (CA2)	+5V	+5V DC power.
AB2 (CB2)	-12V	-12V DC power.
AC2 (CC2)	GND	Signal ground.
AD2 (CD2)	+12V	+12V DC power.
AE2 (CE2)	BDOUTL	Data Output. Implies that valid data is available on lines BDAL0L through BDAL15L and, with reference to the bus master device, that an output transfer is in process. The slave device that responds to the BDOUTL signal must assert BRPLYL to complete the data transfer.
AF2 (CF2)	BRPLYL	Reply. Asserted in response to BDINL or BDOUTL. The signal indicates that input data is available on the BDAL bus, or that output data has been accepted from the bus.
AH2 (CH2)	BDINL	Data Input. When BSYNCL is asserted, BDINL indicates an input transfer from the active bus master. When BSYNCL is not asserted, it implies that an interrupt operation is in process.
AJ2 (CJ2)	BSYNCL	Synchronize. Asserted by the bus master device when it has placed an address on lines BDAL0L through BDAL21L.

TABLE 1
FUNCTIONAL DESCRIPTION OF Q-BUS SIGNALS (cont.)

Bus Pin	Mnemonic	Description
AK2 (CK2)	BWTBTL	Write/Byte. Controls the bus cycle in either of two ways, as follows: 1. Asserted with leading edge of BSYNCL to indicate that an output sequence will follow (DATO or DATOB). 2. Asserted, while BDOUTL is asserted, for byte addressing in a DATOB cycle.
AL2 (CL2)	BIRQ4L	Priority Level 4 interrupt request.
AM2 (CM2)	BIAKIL	Interrupt Acknowledge. Asserted by the processor in response to BIRQL. Causes the device to put an interrupt vector address on the bus.
AN2 (CN2)	BIAKOL	Interrupt Acknowledge Out. Normally asserted to the device having the next-lower priority on the interrupt chain, and appears at BIAKIL input to that device. If the module stores an interrupt request, BIAKOL is negated at the next device.
AP2 (CP2)	BBS7L	Bank 7 Select. Indicates that the address on the bus is for the upper 4K bank. When BSYNCL is asserted, BBS7L will remain active until the addressing of the bus cycle is completed.
AR2 (CR2)	BDMGIL	DMA Bus Grant Input.
AS2 (CS2)	BDMGOL	DMA Bus Grant Output. This processor-generated signal is daisy-chained through all DMA devices on the bus. When asserted, BDGMIL grants bus master status to the DMA device requesting the bus that has the highest priority. If a higher-priority DMA device has no active bus request, BDMGOL passes from that device to the BDMGIL input of the next DMA device. If the higher-priority device has an active bus request, that device inhibits its BDMGOL output. A DMA device requests the bus by asserting BDMRL.
AT2 (CT2)	BINITL	Initialize. Generated by the processor during a power-up or reset operation. Clears all devices on the I/O bus.

TABLE 1
FUNCTIONAL DESCRIPTION OF Q-BUS SIGNALS (cont.)

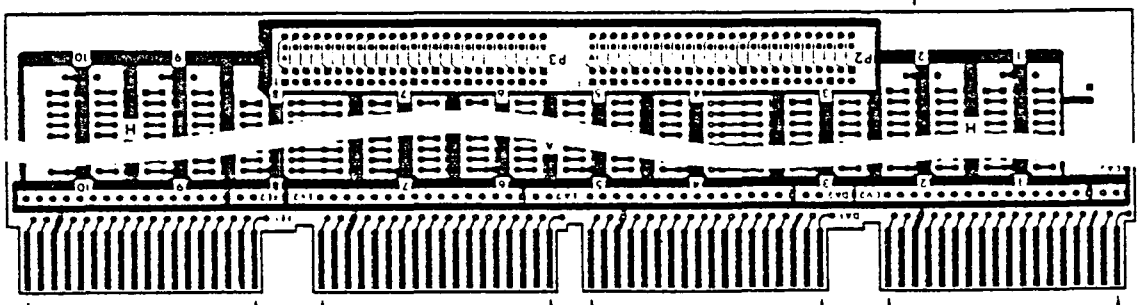
Bus Pin	Mnemonic	Description
AU2 (CU2)	BDAL0L	Bit 0. One of the data/address bus lines used to transfer all address and data information. Bidirectional.
AV2 (CV2)	BDAL1L	Bit 1. Data/Address bit.
BA1 (DA1)	BDCOKH	DC Power OK. Asserted when the DC voltage level is suitable for reliable system operation.
BB1 (DB1)	BPOKH	AC Power OK. Asserted when primary power is within limits assuring reliable system operation.
BC1 (DC1)	BDAL18L	Bit 18. One of the extended address bus lines used to transfer address information.
BD1 (DD1)	BDAL19L	Extended address bit 19.
BE1 (DE1)	BDAL20L	Extended address bit 20.
BF1 (DF1)	BDAL21L	Extended address bit 21.
BH1 (DH1)	SSPARE	Special spare. Not assigned. This pin is available for user connection.
BJ1 (DJ1)	GND	Signal ground.
BK1 (DK1)	MSPAREB	Maintenance spare. Normally connected to bus pin BL1 (DL1) on the backplane.
BL1 (DL1)	MSPAREB	Maintenance spare. Normally connected to bus pin BK1 (DK1) on the backplane.
BM1 (DM1)	GND	Signal ground.
BN1 (DN1)	BSACKL	Bus Grant Acknowledge. Asserted by a DMA device in response to the processor's BDMGOL signal, indicating that the device is now the bus master.
BP1 (DP1)	BIRQ7L	Priority Level 7 interrupt request.
BR1 (DR1)	BEVNTL	External Event Interrupt Request. Using BEVNTL, Line Time Clock interrupts occur every 16-2/3 msec for a 60 Hz line frequency, and every 20 msec for a 50 Hz line frequency.

TABLE 1
FUNCTIONAL DESCRIPTION OF Q-BUS SIGNALS (cont.)

Bus Pin	Mnemonic	Description
BS1 (DS1)	+12B	+12V battery power.
BT1 (DT1)	GND	Signal ground.
BU1 (DU1)	PSPARE	Power spare. Not assigned. This pin is not recommended for use.
BV1 (DV1)	+5V	+5V DC power.
BA2 (DA2)	+5V	+5V DC power.
BB2 (DB2)	-12V	-12V DC power.
BC2 (DC2)	GND	Signal ground.
BD2 (DD2)	+12V	+12V DC power.
BE2 (DE2)	BDAL2L	Bit 2. One of the data/address bus lines used to transfer all address and data information. Bidirectional.
BF2 (DF2)	BDAL3L	Bit 3. Data/Address bit.
BH2 (DH2)	BDAL4L	Bit 4. Data/Address bit.
BJ2 (DJ2)	BDAL5L	Bit 5. Data/Address bit.
BK2 (DK2)	BDAL6L	Bit 6. Data/Address bit.
BL2 (DL2)	BDAL7L	Bit 7. Data/Address bit.
BM2 (DM2)	BDAL8L	Bit 8. Data/Address bit.
BN2 (DN2)	BDAL9L	Bit 9. Data/Address bit.
BP2 (DP2)	BDAL10L	Bit 10. Data/Address bit.
BR2 (DR2)	BDAL11L	Bit 11. Data/Address bit.
BS2 (DS2)	BDAL12L	Bit 12. Data/Address bit.
BT2 (DT2)	BDAL13L	Bit 13. Data/Address bit.
BU2 (DU2)	BDAL14L	Bit 14. Data/Address bit.
BV2 (DV2)	BDAL15L	Bit 15. Data/Address bit.

FIGURE 4
MODULE PIN ASSIGNMENTS

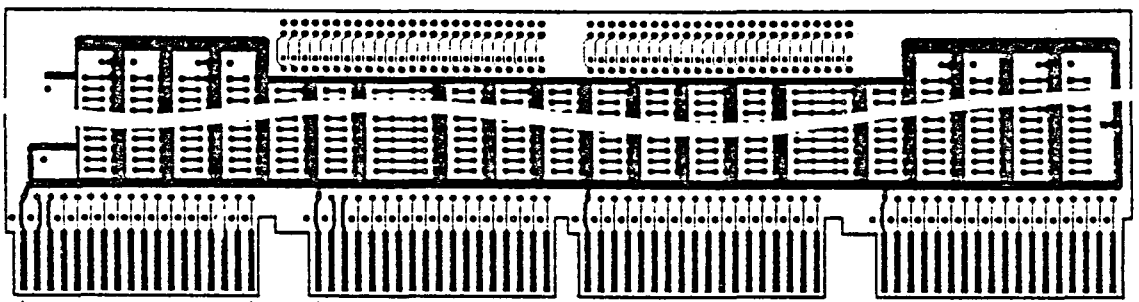
Side 1 — Component Side



72	55	54	37	36	19	18	1

64 = DL1	55 = DA1	46 = CL1	37 = CA1	28 = BL1	19 = BA1	10 = AL1	1 = AA1
65 = DM1	56 = DB1	47 = CM1	38 = CB1	29 = BM1	20 = BB1	11 = AM1	2 = AB1
66 = DN1	57 = DC1	48 = CN1	39 = CC1	30 = BN1	21 = BC1	12 = AN1	3 = AC1
67 = DP1	58 = DD1	49 = CP1	40 = CD1	31 = BP1	22 = BD1	13 = AP1	4 = AD1
68 = DR1	59 = DE1	50 = CR1	41 = CE1	32 = BR1	23 = BE1	14 = AR1	5 = AE1
69 = DS1	60 = DF1	51 = CS1	42 = CF1	33 = BS1	24 = BF1	15 = AS1	6 = AF1
70 = DT1	61 = DH1	52 = CT1	43 = CH1	34 = BT1	25 = BH1	16 = AT1	7 = AH1
71 = DU1	62 = DJ1	53 = CU1	44 = CJ1	35 = BU1	26 = BJ1	17 = AU1	8 = AJ1
72 = DV1	63 = DK1	54 = CV1	45 = CK1	36 = BV1	27 = BK1	18 = AV1	9 = AK1

Side 2 — Solder Side



1	18	19	36	37	54	55	72

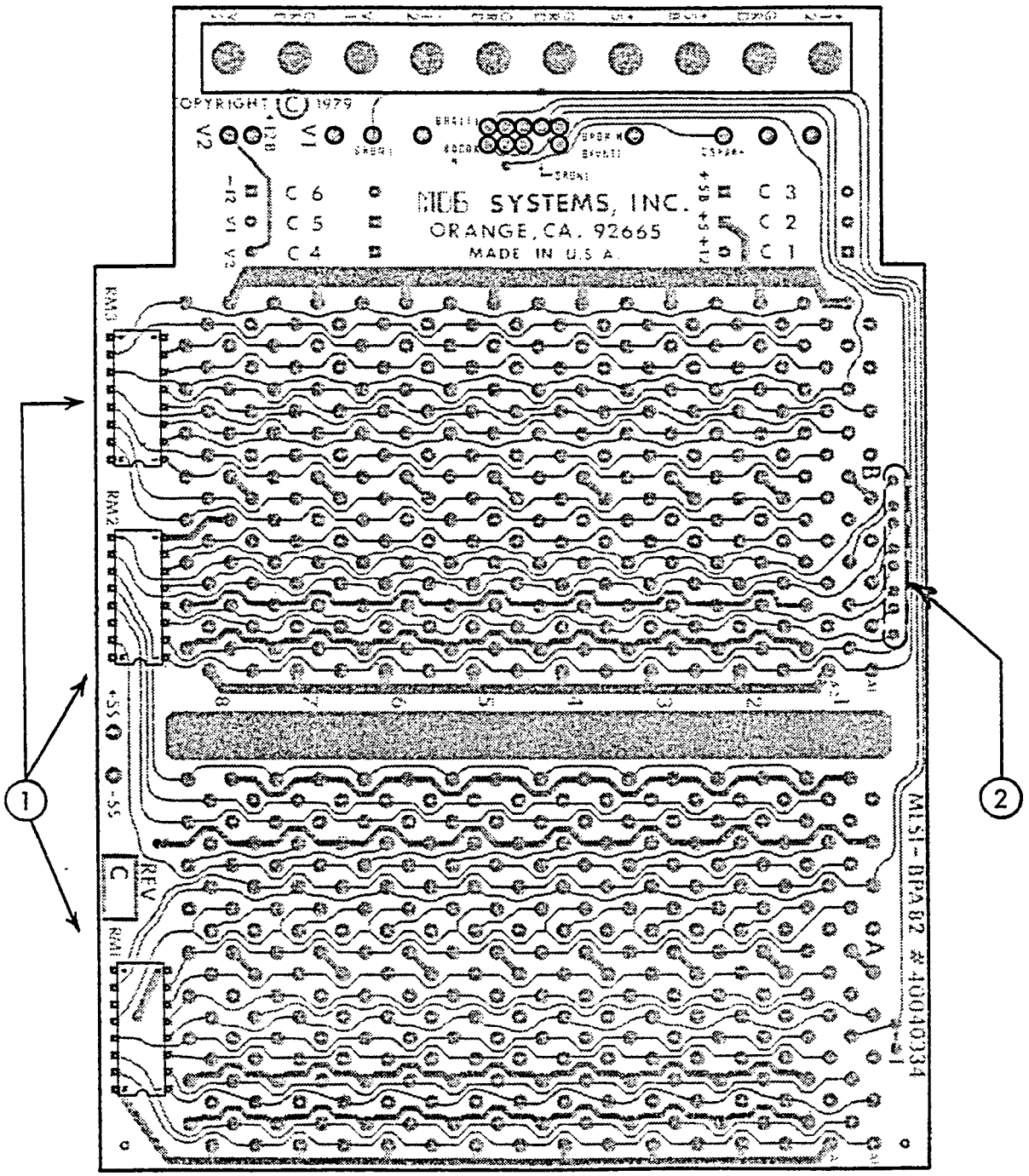
1 = AA2	10 = AL2	19 = BA2	28 = BL2	37 = CA2	46 = CL2	55 = DA2	64 = DL2
2 = AB2	11 = AM2	20 = BB2	29 = BM2	38 = CB2	47 = CM2	56 = DB2	65 = DM2
3 = AC2	12 = AN2	21 = BC2	30 = BN2	39 = CC2	48 = CN2	57 = DC2	66 = DN2
4 = AD2	13 = AP2	22 = BD2	31 = BP2	40 = CD2	49 = CP2	58 = DD2	67 = DP2
5 = AE2	14 = AR2	23 = BE2	32 = BR2	41 = CE2	50 = CR2	59 = DE2	68 = DR2
6 = AF2	15 = AS2	24 = BF2	33 = BS2	42 = CF2	51 = CS2	60 = DF2	69 = DS2
7 = AH2	16 = AT2	25 = BH2	34 = BT2	43 = CH2	52 = CT2	61 = DH2	70 = DT2
8 = AJ2	17 = AU2	26 = BJ2	35 = BU2	44 = CJ2	53 = CU2	62 = DJ2	71 = DU2
9 = AK2	18 = AV2	27 = BK2	36 = BV2	45 = CK2	54 = CV2	63 = DK2	72 = DV2

NOTE 1: For the MLSI-BPA82 backplane, only pins 1-36 apply.
NOTE 2: Lettering of pins excludes G, I, O, W, X, Y, and Z.

TABLE 2
MODULE DIMENSIONS

	Quad	Dual	Single
Height	8.42" (21.40 cm)	8.42" (21.40 cm)	8.42" (21.40 cm)
Width	10.44" (26.50 cm)	5.20" (13.20 cm)	2.44" (6.20 cm)

FIGURE 5
BOTTOM VIEW OF MLSI-BPA82 BACKPLANE

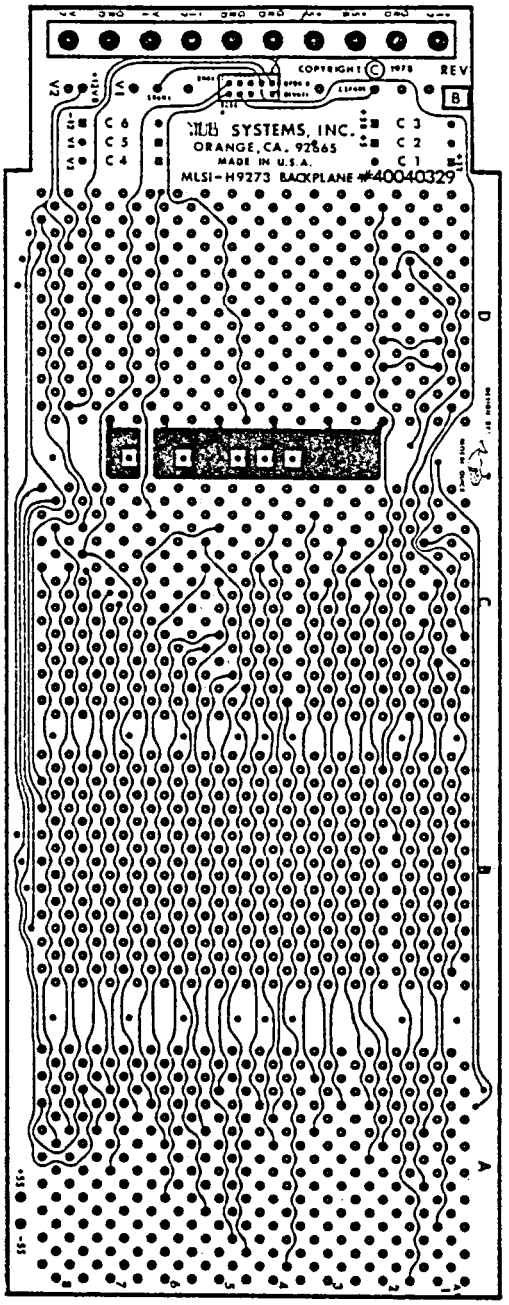


(1) Three (3) removable/pluggable bus termination resistor packs.

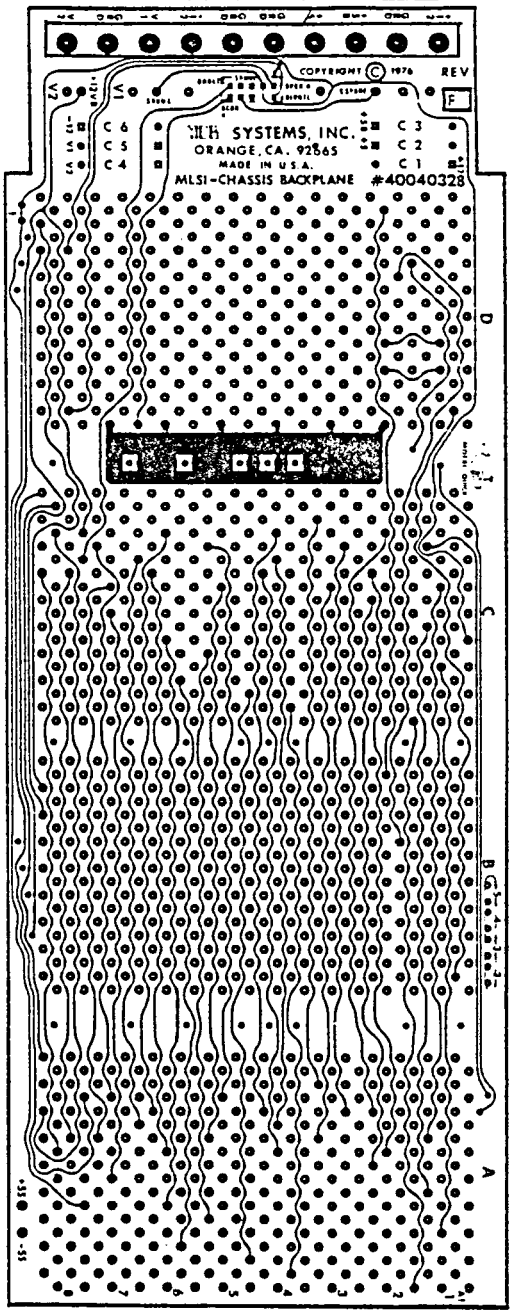
(2) To disable 22-bit addressing lines when using a KD11-F or KD11-HA processor, the etch jumpers must be cut at the location shown above.

FIGURE 6
BOTTOM VIEW OF MLSI-BPA84(-T) AND MLSI-BPA84-A(-T) BACKPLANES

MLSI-BPA84-A and BPA84-A-T



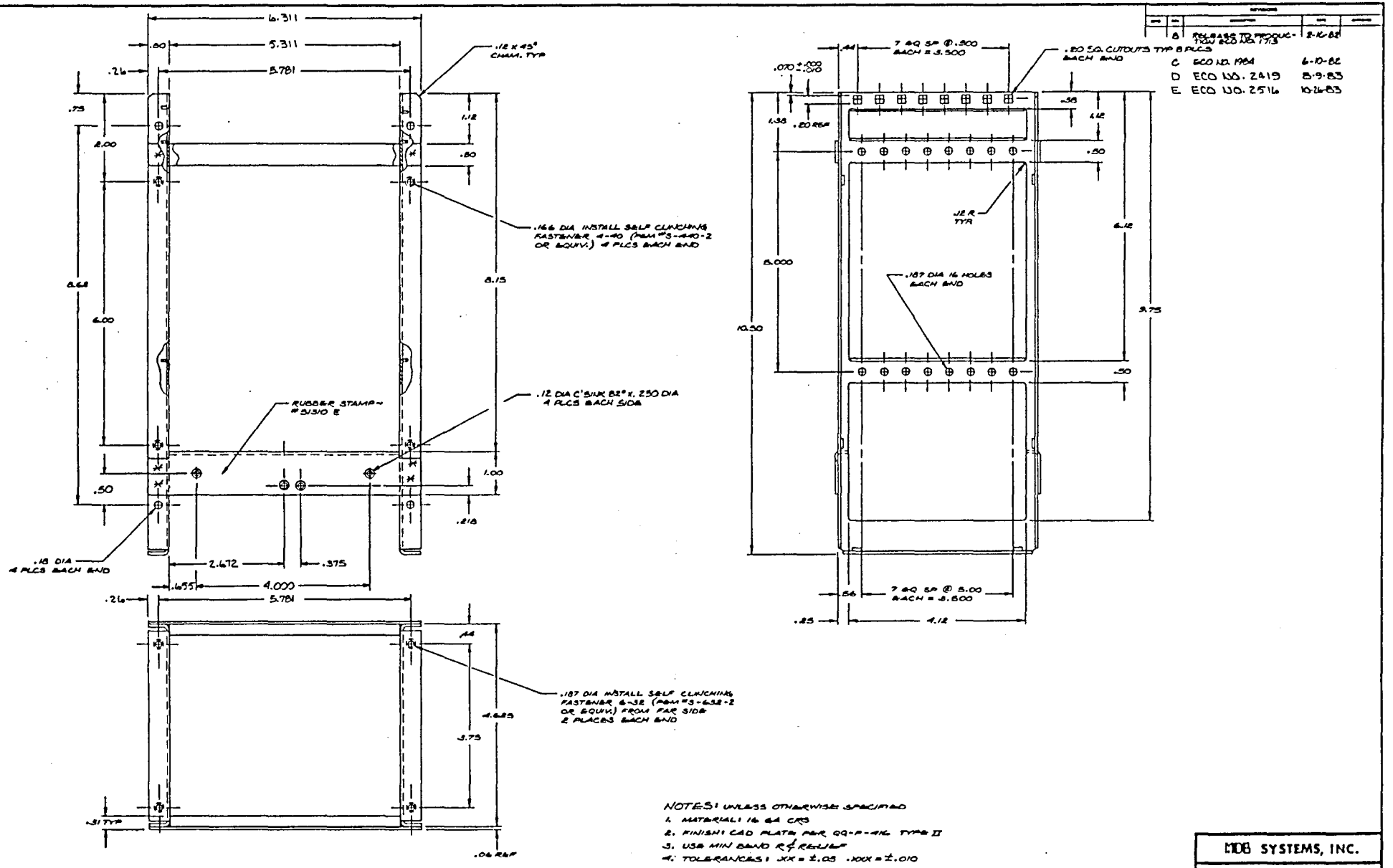
MLSI-BPA84 and BPA84-T



(1) To disable 22-bit addressing when using a KD11-F or KD11-HA processor with an MLSI-BPA84 or BPA84-T backplane, the etch jumpers must be cut at the location shown above. For the MLSI-BPA84-A and BPA84-A-T backplanes, four wire-wrap jumpers (5C1-8C1, 5D1-8D1, 5E1-8E1, and 5F1-8F1) must be removed. These wire-wrap jumpers are not shown above.

NOTE: A jumper wire (not shown) is located between SRUNL and AH1 (Slot 8), and between AH1 (Slot 1) and AH1 (Slot 8). This wire connects SRUNL to the appropriate circuitry on an MLSI-KPV11, or similar module, and provides for the different SRUNL pins of the processor modules.

FIGURE 7
DIMENSIONAL LAYOUT: MLSI-BPA82 BACKPLANE/CARD GUIDE ASSEMBLY

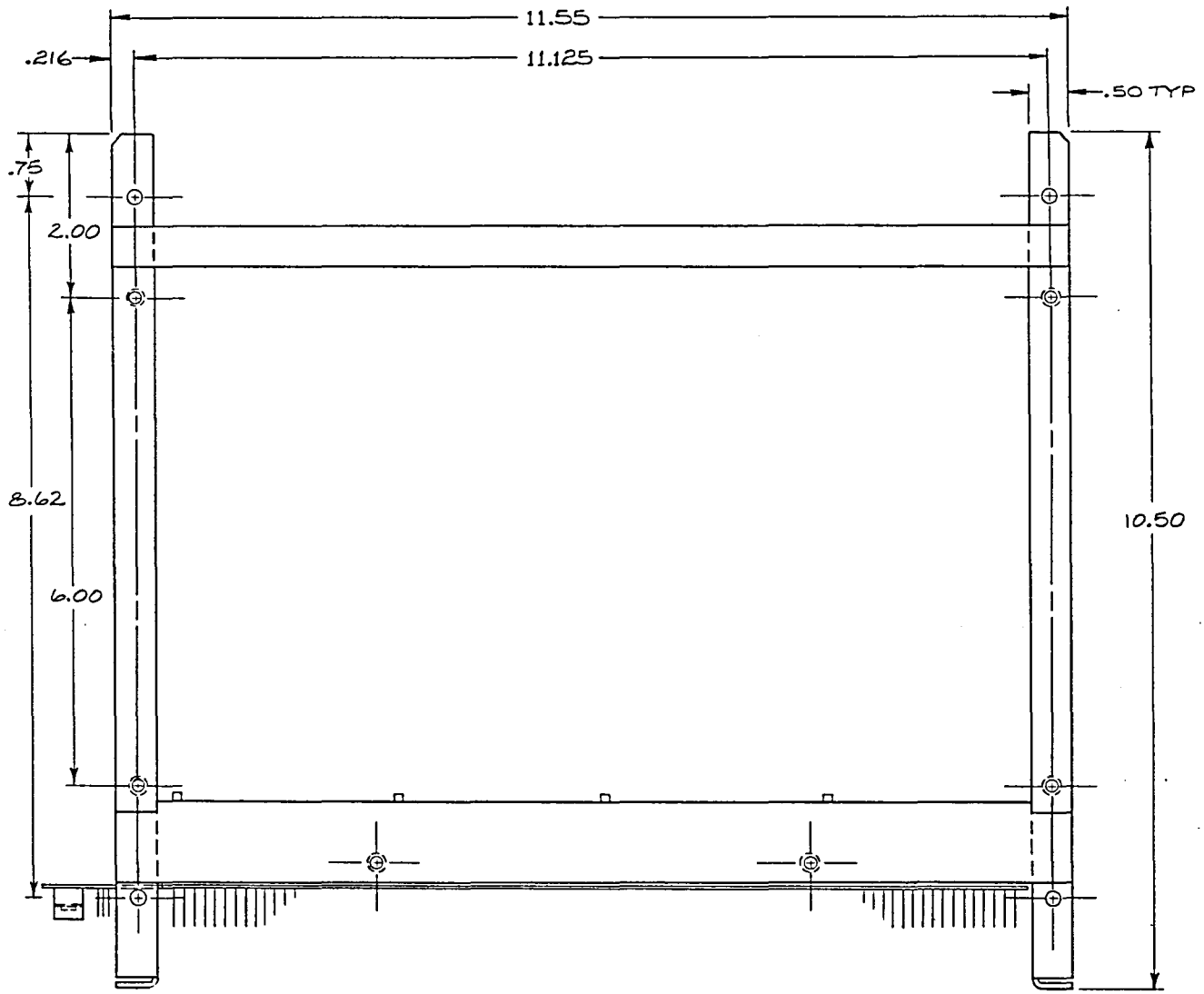


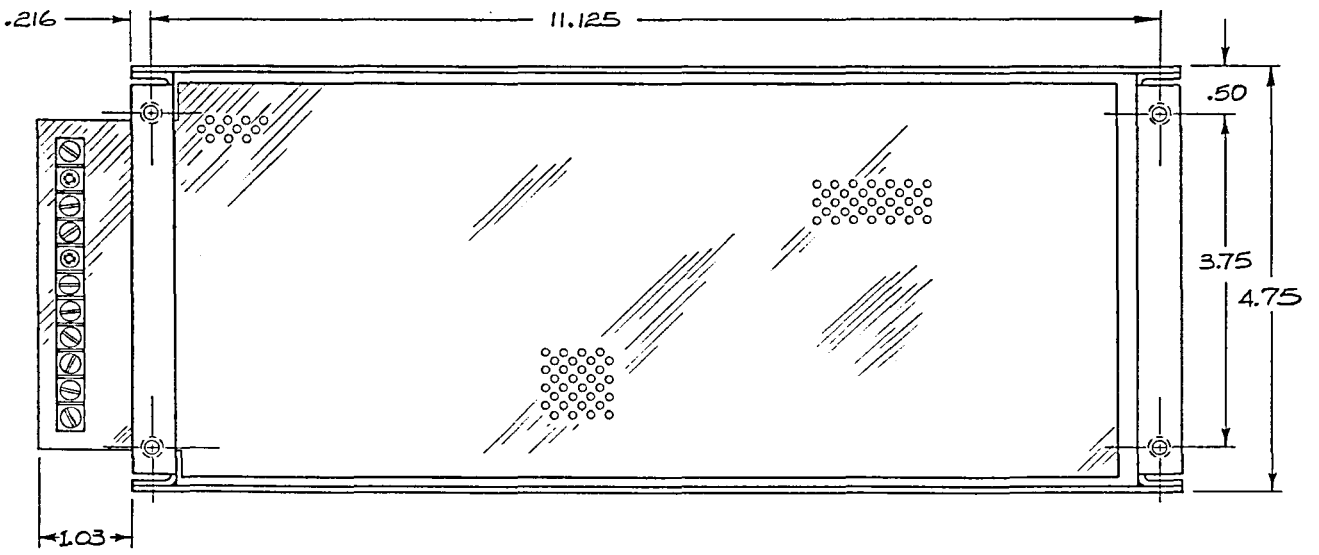
B	RELEASED TO PRODUC-TION ECO NO. 1713		2-16-82
C	ECO NO. 1984		6-10-82
D	ECO NO. 2419		8-9-83
E	ECO NO. 2516		10-24-83

NOTES: UNLESS OTHERWISE SPECIFIED
1. MATERIAL: 16 GA CRS
2. FINISH: CAD PLATE PER QQ-P-416, TYPE II
3. USE MIN BEND R & RELIEF
4. TOLERANCES: .XX = ±.03 .XXX = ±.010

MDB SYSTEMS, INC.	
TITLE: DUAL CARD CAGE	
DATE: OCT 79	SCALE: 1/1
SHEET NO. 1 of 1	DWG NO.: 1502-3/0 E

FIGURE 8
DIMENSIONAL LAYOUT: MLSI-BPA84(-T) AND MLSI-BPA84-A(-T) BACKPLANES





MDB SYSTEMS, INC.	CARD CAGE - INSTALLATION DWG		
DRAWN TWL 11-76	SIZE	FSCM NO. 51648	DWG. NO. 15050329-1 REV. C
ISSUED	SCALE NTS		SHEET 1 OF 1

44040368 | 1 | A

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ECO NO. 1455	12-21-81	
	A	RELEASE TO PRODUCTION ECO NO. 1735	2-25-82	

PARTS LIST

APPLICATION

DO NOT SCALE DRAWING

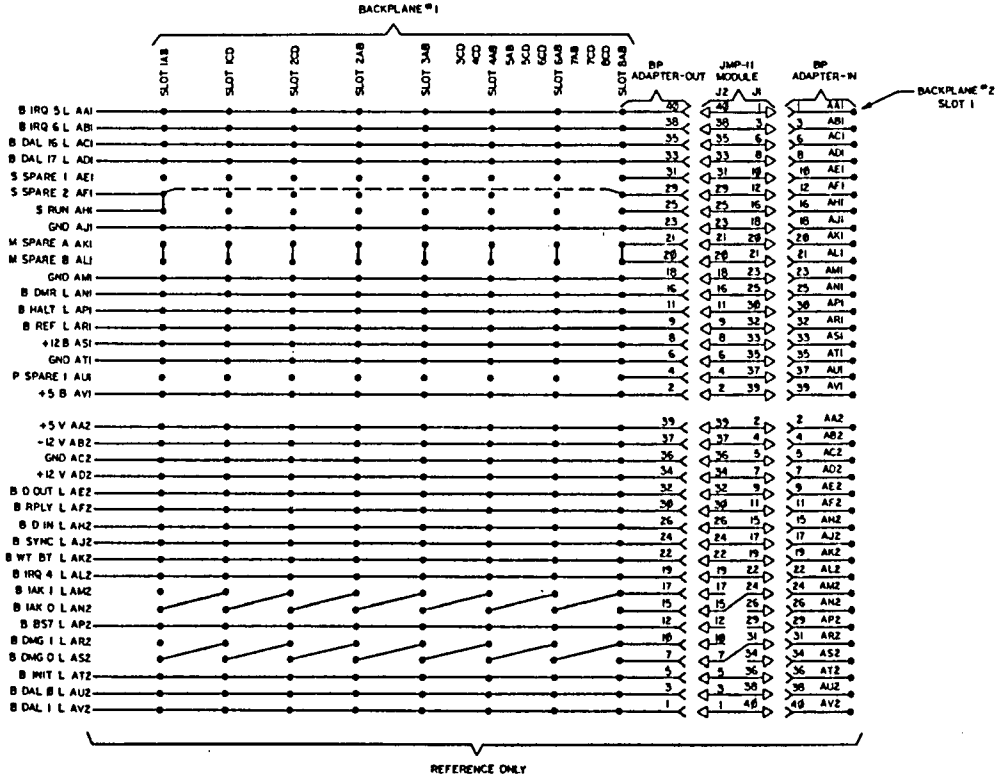
DRAWN	J. MCNEILLY 12-21-81

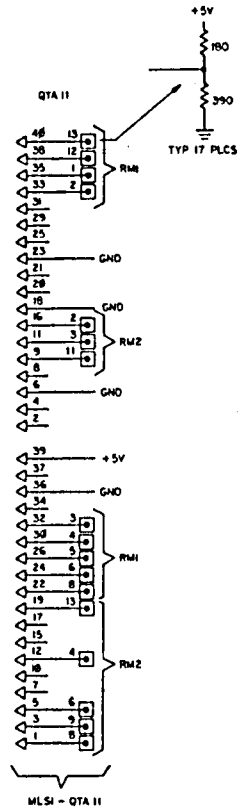
MDB SYSTEMS, INC.

MLSI-QTA11

SIZE	FSCM NO	DWG NO	REV
D	51648	44040368	A

SHEET 1 OF 3

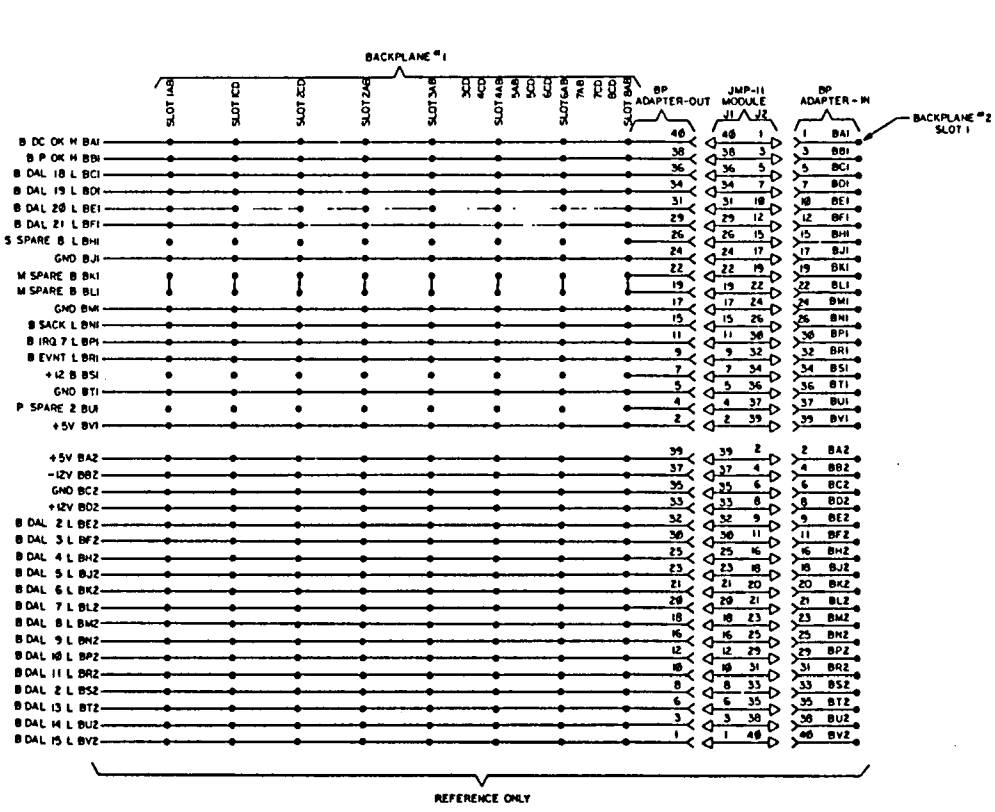


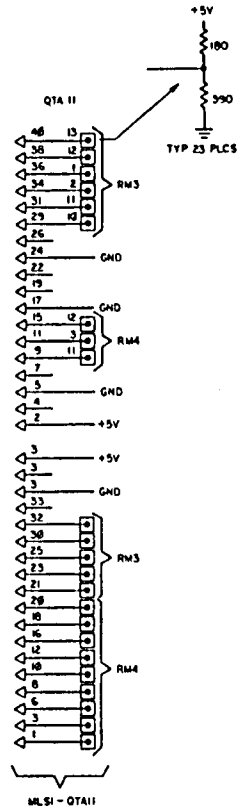


NOTE:
1. JUMPER WIRE FROM SLOT 1AB, PIN AF1, TO SLOT 8AB, PIN AF1, INSTALLED AS AN OPTION.

NOTE:
1. THE FOLLOWING ARE RESISTOR MODULE POWER PIN NUMBERS:
   A. +5V - PIN 14
   GND - PIN 7

MDB SYSTEMS, INC.	SIZE D	PROJ NO 51848	DWG NO 44040368	REV A
DRAWN J.MC.	SCALE		SHEET 2 OF 3	





NOTE:

1. THE FOLLOWING ARE RESISTOR MODULE POWER PIN NUMBERS:
   A. +5V - PIN 14
      GND - PIN 7

DEC SYSTEMS, INC.	SIZE	FSCM NO	DWG NO	REV
DRAWN J.MC.	D	51848	44040368	A
ENGR	SCALE		SHEET 3 OF 3	

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